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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,903	12/10/2003	Seiichi Kawano	JP920030051US1	5795

53493 7590 09/21/2006

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,903	KAWANO ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6-13* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see page of applicant's remarks, filed on 20 July 2006, with respect to claims 9-11 have been fully considered and are persuasive. The rejection of claims 9-11 under 35 U.S.C. 101 has been withdrawn.

Applicant's arguments filed on 20 July 2006 pertaining to art-based rejection of claims 1-3 and 6-13 have been fully considered but they are not persuasive.

Regarding independent claims 1, 8, 9, 10, 12, and 13, applicant has presented the argument that "As opposed to Applicants, Mason's CPU enters an execution halt mode and low-power voltage mode at the same time. See, e.g., col. 8, lines 48-59. In contrast to Mason, Claim 1 is limited to an information processor comprising a mode controlling module that places the CPU into halt mode only after a voltage controlling module has placed the CPU into a low-voltage operating mode" [page 10, applicant's remarks, paragraphs 5 and 6].

The relevant portion of Mason's disclosure is as follows:

"Responsive to the POWERDOWN bit 82, logic circuits in the CPU Interface Chipset 50 de-assert signal CPU_PWR_EN that is connected to the CPU power supply, the frequency generator, or both (Step 205). Depending on the implementation, the de-assertion of CPU_PWR_EN signals the CPU power supply 84 to reduce its output voltage and/or signals the clock generator 86 to reduce its output frequency. **When the power supply voltage and/or frequency are reduced (Step 206)**, Central Processing Unit 12 will stop executing instructions or operate at a greatly reduced speed and transition into a low-power consuming state (Step 207)."

The examiner disagrees with applicant's interpretation of this portion of Mason's teaching. Mason appears to teach that the stoppage of instruction execution occurs when the

power supply voltage and/or frequency have already been reduced. This is further illustrated in Fig. 6. In Fig. 6, Mason clearly teaches that the reduction of voltage/frequency and the halting of instruction execution are two separate and distinct steps, with the halting step following the voltage/frequency reduction step [steps 206 and 207]. Therefore, applicant's assertion that Mason teaches the halting of instruction simultaneously with the voltage/frequency reduction is incorrect. Applicant's amendments to claims 1, 8, 12, and 13 are also insufficient to overcome the prior ground of rejection. The examiner further notes that claims 9 and 10 do contain the amendment which states that the halting occurs after the voltage/frequency reduction.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mason et al., U.S. Patent No. 6,161,187.

Regarding claim 1, Mason discloses an information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode or operating said instruction execution module and an execution halt mode for halting said instruction execution module; said information processor comprising:

a voltage controlling module for causing said instruction execution module to execute a voltage reduction instruction for placing said central processing unit into a low-voltage operation mode in which the operating voltage of said central processing unit is lowered from the

operating voltage in said normal mode when said central processing unit switches from said normal mode to said execution halt mode [col. 5, lines 12-42]; and

a mode controlling module for placing said central processing unit into a low-voltage halt mode in which said instruction execution module is halted under the operating voltage for said low-voltage operation mode after said voltage controlling module places said central processing unit into said low-voltage operation mode [col. 8, lines 48-59].

Regarding claim 2, Mason teaches a halt grant signal allowing the instruction execution module to halt, wherein the mode controlling module places the CPU into a low-voltage halt mode when the module received the halt grant signal [col. 3, lines 45-48].

Regarding claim 3, Mason teaches receiving an interrupt request for returning voltage of an information processor to previous levels, and resuming the execution of instructions [col. 8, line 60 to col. 9, line 9].

Regarding claims 6 and 7, Mason teaches that the CPU voltage may be reduced to zero, or a value greater than zero so that register values in the CPU may remain valid [col. 5, lines 50-60]. As such, the non-zero reduced voltage may be viewed an intermediate voltage operation mode. Alternatively, the non-zero reduced voltage may be viewed as a low-voltage operation mode, and the zero voltage level may be viewed as a voltage reduction mode with voltage lower than the low-voltage operation mode.

Regarding claim 8, Mason also teaches that in addition to reducing the voltage of the information processor, a clock frequency may also be reduced [col. 8, line 52-55].

Regarding claims 9, 10, 12 and 13, Mason teaches the information processor as recited in claims 1 and 8. Mason also teaches that the information processor implements the methods recited in claims 12 and 13. Mason also teaches the signal bearing medium tangibly embodying a program of machine-readable instructions recited in claims 9 and 10.

Allowable Subject Matter

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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